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I am submitting herewith a thesis written by Zuoliang Ning entitled “A High Voltage CCD Sensor Control Chip for the Large Synoptic Survey Telescope (LSST).” I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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A High Voltage CCD Sensor Control Chip for the Large Synoptic Survey Telescope (LSST)

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ABSTRACT

This thesis presents the design of a Sensor Control Chip (SCC) developed to provide the required clock and bias signals for the Large Synoptic Survey Telescope’s CCD imagers. The circuit consists of current-summing DACs followed by trans-impedance operational amplifiers to control the rail voltages of the clock signals and bias voltages. The clocks are input to the SCC through LVDS receivers and converted internally to the required amplitude for driving the CCDs. The ASIC is designed to drive clock signals with 20-V adjustable output voltage swing and a maximum output current of 150 mA. The prototype chip has been fabricated in a 0.8-um BCD-SOI process, and is designed to operate down to 175K. Design techniques used in the ASIC will be presented, along with room temperature and operational temperature test results obtained from prototype chips. Test results have shown that the prototype chip is fully functional and agrees well with simulation results.
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CHAPTER 1
INTRODUCTION AND OVERVIEW

1.1 Introduction

The Large Synoptic Survey Telescope (LSST) [1] is a large wide-field, ground-based astronomical telescope. The telescope, which will be located in northern Chile, will be used as a facility for fundamental physics research, to better understand dark energy and dark fields.

The LSST is designed to provide an image of the full available sky in every three nights. In order to fulfill this goal, it is designed with a wide field-of-view of 10 square-degrees, an exposure time of 15 seconds and a readout time of 2 seconds. The camera will be composed of a mosaic of more than 200 Charge-Coupled Devices (CCDs), each of which has 16M pixels (4K by 4K). The total CCD panel will consist of more than 3 Gpixels of imagers, one of the largest focal-plane CCD mosaics ever built.

First introduced as a memory storage device in 1970, the CCD has revolutionized the fields of science and astronomy [2]. Even though its competitor, the CMOS sensor, has prevailed in the consumer imager market (e.g. mobiles, cameras), in the astronomical imaging arena, where quantum efficiency and image quality is more important, the CCD is still the system of choice.

Closely associated with the CCDs are the electronics and computers to control and handle the huge data stream CCDs generate. As CCDs used in
observatories can be quite different from one another, almost every observatory has developed its own electronic readout and computer systems. In the electronic systems designed for the CCD, an important part is the CCD driver which provides the necessary signals for the CCD to properly function. The Sensor Control Chip, which will be presented in this thesis, is the CCD driver for the LSST, and will provide the required clock and bias signals to the CCDs [3][4].

Because CCDs require a high voltage to produce a reasonable potential well, the clock and bias signals for many CCDs, especially astronomical CCDs, can be as high as several tens of volts. Such voltage levels exceed the normal 5-V or 3.3-V logic level of the control logic, so a level translation must be provided by the CCD driver.

Early CCD drivers were often built with discrete components [5][6] or commercial ICs [7]. As more functionality and better performance are required, many CCD drivers these days are custom ASIC developed with high voltage CMOS/BiCMOS processes [8][9]. With the help of advanced high-voltage CMOS technology, these new clock drivers can build digital functions into the clock driver, have lower parasitic parameters, and consume less power.

1.2 Organization of Thesis

This thesis presents the design and implementation of a high-voltage (capable up to 45 V) CCD sensor-control chip designed for the Large Synoptic Survey Telescope. Test results for the prototype chip are also provided. The thesis is divided into four sections.
Chapter 2 presents an overview of CCD structure and operation. The CCD readout operation is explained to help understand the required function of the SCC. Also included in this chapter is an overview of SCC design requirements and design constraints.

Chapter 3 presents a detailed review of the design of the SCC. Top-level structures and design steps of all major blocks are provided. Detailed circuit analyses and simulation results are also presented.

Chapter 4 presents the measurement results from the prototype SCC. The test setup and results from two different test measurement sets are given.

Chapter 5 presents the conclusion of this work. The accomplishments of this thesis are presented, and suggestions for future research work are proposed.
CHAPTER 2
CCD DRIVER DESIGN OVERVIEW

The CCD driver is the driving component of the CCD controller. As the name implies, CCD driver provides the necessary signals for CCD operation. As stated in Chapter 1, the Sensor Control Chip (SCC) presented in this thesis is the driver for the CCD panel of the Large Synoptic Survey Telescope (LSST).

2.1 CCD Fundamentals

To understand how a CCD driver works, we need to first learn how the CCD works.

The Charge-Coupled Device (CCD) is the most common detectors used in modern telescopes. As the sensor of the telescope, it contains light-sensing units which absorb photons and proportionally generate electrons. Comparing to photographic film, a CCD sensor has a much better linearity, which gives it many advantages over film [10].

2.1.1 CCD Physical Structure

The light-sensing unit used in the CCD is a metal-oxide-semiconductor (MOS) capacitor, which works as a photodiode as well as an electron storage device.

The cross-section structure of the MOS capacitor is shown below in Figure 2-1. When the CCD is exposed to light, photons will first collide with the silicon atoms in the body of the CCD, releasing one electron-hole pair from each
absorbed photon. When a positive voltage is placed on the gate of the MOS capacitor and a negative voltage is impressed on the substrate, the electron field generates a potential well at the silicon surface. When the CCD is in the exposure stage, all the electrons generated by the photons will be kept in the potential well. Although either electrons or holes can be accumulated (dependent on the specific CCD design), electrons are usually considered the charge carrier, and are usually referred to as photoelectrons.

For each photon absorbed by the MOS capacitor, there will be one photoelectron generated. This gives us a way to measure the photons injected in each potential well by measuring the electron numbers. When the exposure stage is over, the photoelectrons will be read out through the n-Channel to a low-noise output amplifier, where the electrons will be sensed and amplified.
2.1.2 CCD Readout

As stated in the previous section, all the photoelectrons are generated in the exposure stage. After the exposure stage, the CCD goes into the readout stage, during which the photoelectrons will be moved sequentially out of the CCD. To accomplish this, a multi-parallel gate structure is used to build the CCD. Each gate corresponds to one of the phases, and has different voltage added on during the readout stage.

A common type of device is the three-phase CCD, whose structure is shown in Figure 2-2. As shown in the Figure, for a three-phase CCD, each pixel is divided into three parts, each of which has its own gate (shown in the figure with different colors). For the following discussion, we will name the three gates Phase 1, Phase 2 and Phase 3 respectively. Same-phase gates of different pixels are connected together in the layout, and are driven by outside clock signals from the CCD driver. In Figure 2-2, the high voltage (+V) is added on Phase 2, and a corresponding potential well is generated under it. Gate Phase 1 and Phase 3 do not have potential wells as they are kept at a low voltage (-V).

By applying different voltages to different gates, we are able to change the potential well’s position in each pixel. As a result, the photoelectrons trapped inside the potential well will be moved as well. There are several voltage sequences that can be used to achieve this goal.
A three-voltage sequence is illustrated in [11], and another two-voltage approach is briefly shown in [8]. The second approach uses only two voltages, which has the advantage of saving one cable channel, and would also make the CCD driver design easier. Figure 2-3 shows a more detailed clock sequence of this approach.

As shown in Figure 2-3, the voltage sequence is periodic with 6 steps. For each of the gate voltages, it is a 50% duty cycle square signal. The three gate signals are in the same amplitude and frequency, but with a 120-degree phase difference between each other. By applying these voltage sequences to the CCD, photoelectrons are moved from one pixel to the neighboring one. As this clock pattern is repeated, the photoelectrons can be moved continuously from one end to the other end of the CCD.

During the exposure stage, one of the pixel gates will be set to high, to create potential well for photoelectrons.

Besides three-phase CCDs, there are also two-phase CCDs and four-phase CCDs, both of which have a similar multi-gate structure, and have gate clocks that work in a similar way.
Figure 2-3 Three-phase CCD Clock Sequence
2.1.3 Parallel Clock and Serial Clock

There are two types of clock signals needed for CCD readout: a parallel clock signal for the CCD sensor (parallel register), and a serial clock signal for the output register.

The effects of the two clock signals are shown in Figure 2-4. The output register line is simply just an extra row of pixels that are hidden from exposure that serves as the transfer row to the output.

Figure 2-4 (a) shows the CCD status after the exposure, where the output register has no photoelectrons (shown in white) and the other pixels have photoelectrons due to exposure (shown in blue).

When the parallel clock is applied to the CCD, it moves one row of pixels up to the output register line each clock cycle. After one row of pixels is shifted to the output register, the serial clock signal is applied to the CCD, and it moves the pixel information out of the CCD (to the CCD amplifier) one-at-a-time.

Because of their functional differences, the two clock signals can behave very differently. The serial clock signal needs a much faster speed than the parallel, so that it can move all the pixels on the output line out before the next parallel shift. The parallel clock, on the other hand, has a much larger load compared to the serial clock, as it needs to drive many more gates (a much larger silicon area). The requirements of the clock signals for the CCD of LSST will be stated in detail in section 2.2.
Figure 2-4 Parallel Clock and Serial Clock

(a) CCD after exposure stage (b) Parallel clock moves one row of pixels to the output register (c) Serial clock moves pixels to the output one at a time
2.2 LSST CCD Driver Design

2.2.1 LSST CCD Structure

As mentioned in Chapter 1, each CCD of the LSST array has 16M pixels (4K by 4K), and needs a total readout time of less than 2 seconds. If only one output is available per CCD, then we would need an 8-MHz serial clock and a 2-KHz parallel clock. However, a parallel structure has been adopted for the CCD, which divides the CCD into 16 segments [1]. In turn, each CCD now has 16 outputs, and the serial clock and parallel clock signal requirements are reduced to 500 KHz and 1 KHz, respectively.

The CCDs of LSST will have a 4-phase parallel clock signal and a 3-phase serial clock signal. For a 4-phase parallel structure, the pixel will always have two of the four clocks at a high state, both during exposure and during readout. This gives a larger “full well” capacity (the maximum photoelectrons a pixel can hold) than a 3-phase structure, which has only 1/3 of a pixel used to hold the electrons. Another benefit is that during the readout stage, there will be two clocks switching from high to low while the other two clocks switch from low to high simultaneously. This gives a balanced transition, which reduces the transient current change on the power line. The serial signals, however, do not need the expanded full well. As they serve as a transfer to the output, their pixels can be made larger. Also, because they have a much smaller clock-to-clock capacitance compared to parallel signals, a balanced transition is not necessary [12].
2.2.2 Design Requirement

The SCC is intended to provide the clock signals as well as DC bias for the CCD. As the prototype CCD device was not available during the SCC design phase, many of the load parameters for SCC are derived from the proposed CCD configurations (pixel size, serial port number, etc.). The specification sheet of the e2V CCD231-84 device [13] is also used for these calculations, as this CCD is very similar the proposed ones in the LSST. As a result, some of the design requirements are as yet not fully established.

The proposed requirements for the SCC are shown in Table 2-1, with currently unknown requirements marked with question marks. Because the CCD clock and bias line voltages can affect the injected noise of the signals read out from CCD, voltage requirements are provided as a range instead of a specific voltage.

Although the serial and parallel clocks do not have the same load or frequency requirements, they do function in a similar way. It is common practice to use the same circuit blocks for these two different clocks to simplify the total design.

Besides the requirements of the CCD, there are also some design constraints that need to be considered in the SCC design. The SCC has been designed with Atmel BCD-SOI process. Although the drain-to-source voltage ($V_{DS}$) can stand several tens of volts, there is a relatively lower voltage limitation on the gate-to-source voltage ($V_{GS}$), as well as body to handling wafer voltage ($V_{BH}$). For example, for the 45-V MOS device, which is widely used in the design,
the $V_{DS}$ limit is 45 V, but the $V_{GS}$ limit is less than 6 V. As we will see in Chapter 3, the process constrains actually put extra limitations on our design.

<table>
<thead>
<tr>
<th>Table 2-1 CCD Signal Requirements</th>
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<tbody>
<tr>
<td><strong>Voltage</strong></td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Minimum Frequency</td>
</tr>
<tr>
<td>Possible Load</td>
</tr>
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</table>
3.1 Block Level Overview

3.1.1 Introduction

The first version of the SCC chip is mainly for the purpose of demonstration and process verification, and it is unnecessary to provide all signals mentioned in Chapter 2 on one chip. To simplify design, only one clock channel and one bias channel have been developed on the first SCC prototype.

The I/O diagram of the SCC prototype is shown in Figure 3-1. Supply voltages and input signals from the backend board are shown on the left side of the diagram, and output signals to the CCD are on the right side. Bias currents established by external adjustable resistors are placed on the bottom side.

3.1.2 Supply Voltage Specification

As shown in the block diagram, the SCC requires multiple supply voltages.

The VDD-1-Switch, VDD-1 and VDD-1_L in the diagram are all supply voltages for the clock channel. VDD-1 and VDD-1_L are two floating power supplies that are 5 V apart, which provide power for the clock driver's upper channel. The VDD-1-Switch pin is expected to have a large current flowing through it and is connected to VDD-1 outside the chip and connected to the clock drivers inside the chip.
Figure 3-1 SCC I/O Diagram
VDD-2 and VDD-2_L are floating voltage supplies 5 V apart for the bias channel. VDD-3 is a 5 V power supply rail used for all 5-V devices in the SCC.

In addition to multiple supply voltages, separate grounds were also employed for the SCC. The 5V_GND is the ground for 5-V devices, while the 45V_GND is the ESD ground for the low-current 45-V ESD devices. The Switch_GND is used as the ground for the clock drivers. Because large transient currents will flow through Switch_GND during switching, it is necessary to keep the Switch_GND separate from the other two grounds.

The sub-block diagram of the SCC is shown in Figure 3-2. The digital input signals are input to the shift cells, and are used to set the input bits of the three DACs (Digital-to-Analog Converters). By controlling the DAC inputs, the bias
signal voltage and clock signal amplitude can be adjusted. The LVDS signals are input to the clock driver and translated to a single-ended clock signal.

3.2 Clock Rail Voltage Structure

As stated in Chapter 2, the SCC provides clock signals for the CCD. Because the voltages of the clock signals are related to the injected noise of the CCD signals being read out, all the clock voltages are required to be adjustable. As shown in section 2.2.2, the clock voltages are required to swing between a 0-2.5 V lower rail and a 15-25 V upper rail. Similarly, the DC bias lines will also affect the noise and power dissipation of the CCD, and bias values up to 32 V may be required.

The adjustable voltage structure of the clock signals is shown in Figure 3-3. Two source followers are used to provide supply rails for the clock drivers. By

![Figure 3-3 Clock Channel Voltage Structure](image)
changing the gate voltage of the source followers, their source voltage will also change with a voltage difference of $V_{GS}$.

Because all switching currents will flow through the two source followers, they must be capable of large transient currents (over 100 mA), which requires a large total width ($W$). The $V_{GS}$ of the source follower should not be too high, which requires a large width-to-length ratio for the two MOSFETs. As a result, the two MOSFET source followers are designed with a $W = 4,000 \mu m$ and a large width-to-length ($W/L$) ratio of 2667 ($L=1.5 \mu m$).

### 3.2.1 Source Follower Voltage Control

To change the gate voltage of the source follower, a trans-impedance configured operational trans-conductance amplifier (OTA) [14] is used together with a current-summing digital-to-analog converter (DAC). By controlling the digital input of the DAC, we can control the DAC’s output current, which in turn changes the output voltage of the OTA, which is also the gate voltage of the source follower.

The OTA and DAC structures are shown in Figure 3-4. Since the gate of the source follower has very high input impedance that can be ignored in most cases, the load of the OTA is represented as a capacitor. To simplify the following discussion, power rails VDD-1 and VDD-1_L are simplified as Vdd and Vss, respectively. As stated in section 3.1.2, Vdd and Vss are floating voltage supplies that are 5 V apart.
For an ideal OTA, both inputs of the OTA will have the same voltage when negative feedback is applied. The output of the OTA in this circuit configuration would be:

\[ V_{OUT} = V_{ss} + I_f \times R_f \]  

(3-1)

From the equation, the output voltage is determined by the lower rail voltage \((V_{ss})\), DAC’s output current \((I_f)\), and the OTA feedback resistor \((R_f)\). Since \(V_{dd}\) and \(V_{ss}\) are the power rails for the OTA, they will also be the upper and lower limits of the output voltage. As the output voltage span is known, the total number of bits of the DAC can be derived from the expected voltage change per step.

For this system, a 5-V output range with less than 100-mV step change is desired. Suppose the DAC has \(n\) bits, then we should have:

\[ 2^n - 1 \geq \frac{5V}{100mV} = 50 \]  

(3-2)

Because \(n\) needs to be an integer, we have \(n=6\), and a 6-bit-DAC is selected for this application. The corresponding voltage change per step is:
\[
\frac{5V}{2^6 - 1} \approx 79.4\text{mV}
\] 

(3-3)

### 3.2.2 DAC and Shift Cell Structure

As in Figure 3-4, the DAC works between a 5-V rail and ground. Because the 5-V device has a much smaller layout size than the 45-V device, the low-voltage DAC saves much layout area.

As we do not require a very precise DAC for this application (i.e., the clock signal voltage does not need to be very precise), a simple current-summing DAC is used for this design that is shown in Figure 3-5.

The bias current in Figure 3-5 is set by an output resistor to 4 µA. For ideal current mirrors, the maximum current can be obtained when all input bits (Bit0 to Bit5) are at 0 V (or low). The maximum output current would be:

![Figure 3-5 Upper Channel 6-bit DAC Structure](image)
\[ I_{f,\text{max}} = \frac{4\mu A}{8} \times 63 = 31.5\mu A \]  
\[ (3-4) \]

The DAC output current is mirrored to the OTA by a 45-V-device current mirror. In this way, the low-voltage DAC is isolated from the high voltage OTA.

From Equation 3-1, since \( V_{\text{ss}} \) is fixed, to obtain a 5-V range the feedback resistor needs to be

\[ R_f = \frac{5V}{I_{f,\text{max}}} = \frac{5V}{31.5\mu A} \approx 158.7k\Omega \]  
\[ (3-5) \]

A medium-speed shift cell is used to sequentially shift the DAC bits into the chip. The diagram of the shift cell is shown in Figure 3-6 that includes one multiplexer and two D Flip-Flops. Each shift cell corresponds to one DAC bit, and they are connected in a sequential way to make a serial-input, serial-output structure. To program the chip, one must exercise the Shift_Clk when the desired

![Figure 3-6 Shift Cell Diagram](image-url)
data bit is at the Data_In pin. Each falling edge will shift one bit into the SCC chip. After all bits are shifted in, we exercise the Data_Clk once to load the bits to the DACs. The Select signal can be used to read the DAC input digits nondestructively back to the shift cells, and the result digits can then be shifted out using Shift_Clk for verification purposes.

### 3.2.3 Operational Transconductance Amplifier (OTA) Structure

To obtain the maximum output range, a simple OTA structure is used for the upper rail. The diagram for the OTA is shown in Figure 3-7. From Figure 3-4, if functioning properly, both of the OTA's input voltages will be equal to Vss. A PMOS input pair is used to ensure Vss is within the common-mode input voltage range.

An important parameter shown in the Figure 3-7 is IBias, which is the bias...
current for the OTA. As with other bias currents of the SCC, IBias is established using an off-chip resistor. The numbers next to the MOSFET in the figure show the gain ratio of the current mirror. For example, from the current mirror ratio, we would know the tail current for the PMOS input pair is twice IBias.

The IBias has two important influences on the OTA. First, it determines the maximum output current of the OTA. Because the inverting input and the non-inverting input of the OTA are at the same voltage, the tail current will be split equally. Since the tail current is 2×IBias, each PMOS device of the input PMOS pair will have a current equal to IBias flowing through it. As another 1:2 current mirror is used at the output stage, the maximum current would be equal to 2×IBias.

IBias will also determine the power consumption of the OTA. In the worst case, when I_i is maximum, the power consumption of the OTA would be approximately,

\[ P = (Vdd - Vss)(6 \times IBias + I_{f,max}) + Vss(IBias + I_{f,max}) \]
\[ = 5 \times (Vdd - Vss) \times IBias + Vdd(IBias + I_{f,max}) \]  \hspace{1cm} (3-6)

These two influences make setting the design IBias value a little tricky. To lower the power consumption, in order to relieve the thermal control burden (within LSST), we need IBias to be as small as possible. However, the output current needs to be large enough to provide sufficient feedback current, which requires IBias to be reasonably large.

To evaluate the influence of IBias on the OTA performance, simulations of OTAs with different IBias current values were performed. Figure 3-8 shows the
Figure 3-8 OTA’s Output and Inverting Input Voltage
(a) IBias of OTA set to 30uA (b) IBias of OTA set to 60uA
corresponding OTA output voltage and inverting-input voltage when sweeping DAC current (i.e. feedback current for OTA) from zero to its maximum current for two OTAs with 30 µA/60 µA IBias currents. As we can see, the OTA with a larger IBias value can afford higher output current, which results in better linearity with high DAC currents. Based on the simulation results, the OTA bias current IBias is set to 60µA.

3.3 Clock Driver

3.3.1 Floating Current Source

As shown in Figure 3-9, one floating current source and two current switches are placed between the upper and lower rails. The floating current source provides a bias current to keep the source followers on, which would speed up the voltage-change rate. Two identical current switches are used together to provide the clock signal for the CCD. The two switches are identical.

Because there is no specific requirement for the bias current source, we used a simple floating current source for the structure. As shown in Figure 3-10,

![Figure 3-9 Clock Driver and Bias Circuit Architecture](image-url)
the floating current source we used has asymmetrical current flowing through the upper and lower rails. However, for this application the design is adequate to simply provide bias current for the two source followers. As with all the other bias currents we talked before, the $I_{FS}$ level is established off-chip by a resistor and can be easily adjusted.

### 3.3.2 Clock Driver (Current Switch)

As stated in Chapter 2, the clock driver translates the LVDS (low-voltage differential signaling) signal to serial/parallel clock signals for the CCD sensors.

As shown in Figure 3-11, the translation of the LVDS signals can be divided into 3 steps. First, the LVDS signals will be sent to two receivers built inside the SCC. The LVDS signals are connected to the receivers’ inputs in a complementary way, and will be translated to two 0-5 V differential signals. The
new differential signal pair then goes into a 5-V buffer. Finally, the buffered signals are transferred to the clock driver and translated to a desired clock signal.

The LVDS signal is a differential signal transmission standard widely used for high speed, short distance data transmission [15]. The term “differential” means it will transmit two opposite-phase signals, which will be compared at the receiver to generate the final single-ended signal. The common-mode input voltage for the differential pair is 1.2 V, and the differential voltage of the input pair is about 350 mV.

The structure of the LVDS receiver is shown Figure 3-12. The receiver also adopted an OTA structure. Unlike the OTA in section 3.2.3, the receiver used a simple current mirror for the tail current. Because the power supply of the receiver is 5 V, all devices used in the receiver are 5-V devices. I_{out} is set to 20 µA, and is established by an external resistor.

The buffer is used here to boost the input signal, and will provide larger source or sink current capable of driving larger load.
The clock driver schematic is shown in Figure 3-13. Bias current for the OTA is set to 75µA using an external resistor. The current mirror for the bias current is not connected to the upper rail, but to the +15 V rail. This ensures the bias current will stay constant when the upper rail voltage changes.

Recall from Chapter 2 that the selected manufacturing process requires the MOSFET's gate-to-source voltage $V_{GS}$ be below 6 V. To comply with the requirement, two input level shifters are used before the OTA input pair. The level shifter would shift the input voltage up. The $V_{GS}$ of M11 (M12) needs to be at least 1.3 V to have a 75-uA current flowing through the device. This means the level shifter would at least shift the input voltage up by 1.3 V. And a higher input voltage on M3 and M4 would allow their source voltages to be higher.
Assume the lower rail voltage of the clock driver is $V_L$. Suppose the input on M11 is 5 V and input on M12 is 0 V, so the tail current should all flow through M3. In this case, the source voltage of the M3 and M4 would equal to:

$$V_{S3} = V_L + V_{GS1} + V_{SD3}$$  \hspace{1cm} (3-7)

In Equation 3-7, $V_{GS1}$ stands for the gate-to-source voltage of M1, and $V_{SD3}$ stands for the source-to-drain voltage of M3. For a given tail current, the $V_{GS1}$ and $V_{SD3}$ should roughly track one another. As a result, the source voltage of M3 should almost increase linearly with the lower rail voltage. A simulation shown in Figure 3-14 has confirmed this conclusion.

Because the source voltage of M3 and M4 increases with the rail voltage and there is a $V_{SG}$ limit for M3 and M4, there would be an upper limit for the lower rail voltage. The upper limit for the lower rail from the transient simulation is
around 5.3V. Further simulation with device corner models shows the gate of the lower source follower (set by lower DAC) is required to stay below 3 V, for $V_{SG}$ of M3 and M4 to stay in the safe range.

The classical inverter architecture [16] would require a $V_{GS}$ voltage nearly equal to the upper rail and lower rail voltage difference, which is over 6 V in this design. Thus, an OTA structure was adopted instead of an inverter structure.

A bias current of 75 µA is used for the OTA structure. A 20:1 current mirror is used to provide 1.5 mA for the tail current, followed by a 1:50 current mirror used in the OTA structure to obtain the desired 150 mA output current (75 mA per switch). Since $I_{Bias}$ can be adjusted outside the chip, we can adjust the output current externally if necessary.
The simulation results of the clock driver are shown in Figure 3-15. As shown in the figure, the edges of the output clock are asymmetrical. The slew rate of the rising edge is larger than that of the falling edge; as a result, the rise time is smaller than the fall time.

As we can learn from the schematic, when the output voltage is rising, the clock driver is sourcing current to the load capacitance, and we expect the PMOS current $I_{M8R}$ to be as high as possible while the NMOS current $I_{M6R}$ is as low as possible. When the output voltage is falling, the clock driver is sinking current, and we want $I_{M8F}$ to be low and $I_{M6F}$ to be high. The output current simulation results for M6 and M8 are shown in Figure 3-16. Comparing the rising edge with the falling edge, we can see the $I_{M6F}$ is smaller than $I_{M8R}$, and $I_{M8F}$ is larger than $I_{M6R}$. This makes the clock driver’s sourcing current larger than the sinking current, and causes the asymmetrical behavior.

The fundamental reason for this asymmetrical behavior is the imbalance between the PMOS and NMOS devices. As M6 and M8 have large layout areas, their gate-to-source capacitances cannot be ignored. Simulations show that the PMOS device has about two times more gate-to-source capacitance than the NMOS, and it also requires a higher $V_{SG}$ than the NMOS $V_{GS}$. These differences cause the PMOS to take a longer time to turn off, and cause the $I_{M8F}$ to be larger than $I_{M6R}$. 

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Figure 3-15 Clock Driver Output Simulation
(a) Output waveform overview (b) Output rising edge (c) Output falling edge
Figure 3-16 Clock Driver Output Simulation Analysis
(a) Output rising edge current (b) Output falling edge current
3.4 Bias Channel

A bias channel is required to provide all the necessary bias voltages for the CCD. As mentioned in Chapter 2, the bias signals need to be adjustable for this design. Since the load of the bias channel can be considered purely capacitive, and we do not need a very precise value for the bias signal, a structure same as that shown in Figure 3-4 is used for the bias channel. The Vdd and Vss for the bias channel OTA are separate from those for the upper OTA, as the bias voltage can be quite different with respect to the upper gate voltage.
CHAPTER 4
MEASUREMENT RESULTS

4.1 SCC Physical Layout

The SCC is fabricated using the Atmel SmartIS BCD-SOI process. The SmartIS is a high-voltage BiCMOS SOI process that is quite suitable for this application. The overall physical dimensions of the die are 3 mm by 2 mm.

The micrograph of the SCC is shown in Figure 4-1, and an overview of the floor plan is illustrated in Figure 4-2. The SCC has a total of 44 pads, and due to the large current flowing through the chip, some high-current signals need more than one pad. The pad and ESD layouts take large layout areas, and the perimeter of the chip is barely enough to handle these I/O requirements. As a result, this SCC prototype is not limited by circuit area, but rather the required total number of I/O pins.

4.2 Test Setup

4.2.1 Test System Setup

A test system was built for the SCC chip to verify its performance. Because the SCC is designed to be operated under −100°C, the test system for the SCC had to be capable of providing the necessary low temperature test conditions. Because bias currents for the SCC need to be adjusted during the test, an external board placed outside the temperature chamber was also necessary.
Figure 4-1 Sensor Control Chip Micrograph

Figure 4-2 Sensor Control Chip Floor Plan
The test system also needed to transmit the DAC setting to the SCC through the serial programming interface and provide the LVDS signal for clock switching.

The test system diagram is shown in Figure 4-3. The remote test board hosted the SCC chip, and was placed in the temperate chamber during the low temperature testing. An interface board was used outside the test chamber to provide the bias current signals for the test board. It also worked as an interface between the National instruments (NI) measurement system and FPGA board, and translated 3.3-V digital signals from FPGA to 5-V signals that were compatible with the sensor control chip.

The FPGA handled all the SCC configuration work. It is controlled by the computer and NI instruments and generated digital signals and fast LVDS signals for the SCC when a command from the computer was received. It also read back the SCC DAC digits, compared them with the computer settings, and sent the results back to the computer. A Xilinx Spartan-3A development board was used for the test setup, which could provide LVDS signals and digital signals up to
speeds of 50 MHz.

The NI instruments included a NI-6536 interface card installed in a NI-PXle-1026Q chassis [17]. The computer and NI instruments communicated with the FPGA board through the interface board, and provided an easy-to-use GUI for the user to set the DAC values and control the LVDS signals. It also read back DAC setting results from the FPGA, and gave warnings when an error occurred. By connecting other measuring instruments to the NI test system, we were able to set up automated tests for the SCC.

Details of the test setup are furthered explained in the Appendix. Included are pictures of the test setup, remote test board, and interface board.

4.2.2 Test Supply Voltage Setup

As mentioned in section 3.1.2, multiple voltages are needed for the SCC. To simplify the test system, the voltage supplies for the upper channel and bias channel were tied together (i.e., VDD-1 and VDD-2, and also VDD-1_L and VDD-2_L), and were set to 10 V and 15V during the early stages of the room-temperature testing, and 15 V and 20 V for all the other tests.

4.3 Test Results

4.3.1 Single Chip Test

A single chip was used for functionality test of the SCC; both clock channel and bias channel.
Figure 4-4 shows the measured bias channel output voltage with bias DAC bits sweep from 0 to 63. As mentioned in 4.2.2, the power supplies for the bias channel were set to 15 V and 20 V during the measurement. As shown in the figure, for the same DAC bits, the bias voltage at −100°C was larger than that measured at room temperature. This was caused by the feedback resistor of the bias channel OTA, which had a negative temperature coefficient (i.e. a larger resistance at lower temperature). As a result, for the same DAC current, the voltage drop over the feedback resistor at −100°C was larger than that at room temperature. With proper biasing for the DAC, the bias channel output voltage was able to cover the complete 5-V range at a −100°C temperature. The linearity of the bias channel is affected by the fact that we used a simple layout scheme.
for the DAC. As shown in Figure 4-5, the worst case of the differential nonlinearity (DNL) happens at code 32, when the DAC bits change from “011111” to “100000”, which lead to the largest current mirror to be turned on and all the other current mirrors to be turned off. Since bias-signal linearity is not very critical for a CCD, the result is still acceptable for this application.

The clock channel test result at low temperature is shown in Figure 4-6. An onboard 100-pF ceramic capacitor was connected to the clock output to simulate the serial clock load capacitance. The actual measured capacitance was 120 pF at −100°C. The difference comes from parasitic board capacitance and capacitance changing due to temperature. As shown in the figure, the output voltage switches with the LVDS input signal, which is set to 1 MHz. Comparing with Figure 3-15, we can see a similar asymmetrical behavior between the rising

![Figure 4-5 Differential Nonlinearity of Bias Voltage at -100 °C](image)
edge and falling edge, which shows the simulation has good agreement with the test results.

The simulation result for a 100-pF load at low temperature is shown in Figure 4-7. And the comparison between test and simulation results is shown in Table 4-1. The measured result had a higher lower-rail voltage than the simulation result, which might be caused by a larger $V_{SG}$ for the PMOS source follower. The measured rise time result is similar to the simulation results, while the fall time is longer than the simulation. Generally speaking, though, the test results are close to what we expected, and the clock channel is switching properly with the input LVDS signal.

To verify the upper and lower DACs' functionality, different DAC values were
Table 4-1 Low Temperature Simulation and Test Results

<table>
<thead>
<tr>
<th></th>
<th>Simulation Results</th>
<th>Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage</strong></td>
<td>1.17V — 14.03V</td>
<td>1.4V — 13.8V</td>
</tr>
<tr>
<td><strong>Rise Time</strong></td>
<td>27.9ns</td>
<td>23ns</td>
</tr>
<tr>
<td><strong>Fall Time</strong></td>
<td>33.4ns</td>
<td>40.3ns</td>
</tr>
</tbody>
</table>
input to the system and the corresponding clock waveforms were recorded. Figure 4-8 shows the output signals measured at maximum DAC value and a mid-range DAC value. As shown in Figure 4-8, the top and bottom voltages of the output clock signal vary with different DAC values, but the shape of the waveform is consistent.

Table 4-2 shows the serial clock output results at minimum DAC values for different chips. The chip-to-chip variation for the output clock bottom voltage is large. The variations of the top voltage, rise time and fall time also exist, but not as large as the bottom voltage changes.

Figure 4-9 shows the parallel clock test waveform. The parallel line was attached to a 100-nF load capacitor, whose actual capacitance changes with the temperature. Due to a much larger load capacitance on the clock line, the output clock signal showed a much longer rise and fall time (around 8.6 \( \mu s \)). The off-chip bias resistor was set to provide a 150-mA current at the output.

<table>
<thead>
<tr>
<th>Chip</th>
<th>Voltage</th>
<th>Rise Time</th>
<th>Fall Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip 3</td>
<td>1.4V – 13.8V</td>
<td>22.5 ns</td>
<td>38.5 ns</td>
</tr>
<tr>
<td>Chip 4</td>
<td>1.9V – 13.9V</td>
<td>25.5 ns</td>
<td>43.5 ns</td>
</tr>
<tr>
<td>Chip 6</td>
<td>1.4V – 13.8V</td>
<td>23 ns</td>
<td>40.3 ns</td>
</tr>
</tbody>
</table>

Table 4-2 Low Temperature Simulation and Test Results

Test results obtained at -100°C, both DACs are set to minimum.
Figure 4-8: Serial Clocks with Different DAC Values

(a) DAC values at maximum (b) DAC values at mid-range
Since the load is purely capacitive, the output current can be derived from the rise and fall slope of the waveform. The actual load capacitance measured at −100°C was 76 nF, and the maximum slope of the rise and fall edge was about 1.8 V/µs. The derived output current is:

$$I = C \frac{dV}{dt} = 76\text{nF} \times 1.8\text{V/µs} = 136.8\text{mA}$$  \hspace{1cm} (4-1)$$

This output current is 8.8% smaller than the expected 150 mA. The difference might come from the 1:50 current mirrors of the clock driver, which has too large a ratio to provide a perfect matching.
4.3.2 Crosstalk Test

The crosstalk testing was performed to test the interaction between two or more neighboring clock signals on the same CCD sensor.

We have briefly explained the CCD structure in Chapter 2. For clock signals driving the same CCD, their gate structures are built next to each other on the CCD. Such a structure produces cross-coupling capacitances between neighboring signal lines. The coupling capacitance will cause the clock signals to interact with each other and cause signal crosstalk. From the crosstalk test, we studied the effect of crosstalk and evaluated its influence on the system performance.

Because the prototype CCD was still not available to properly study the crosstalk, the load in the test needed to have electrical characters similar to those of the CCD. A typical model for one pixel of a three-phase CCD is shown in Figure 4-10. The Clock Main, Neighbor 1 and Neighbor 2 signals are identical. To simplify the analysis, the cross-coupling capacitor between Neighbor 1 and Neighbor 2 is omitted and combined with their ground capacitance, and we will only consider the influence of the Main Clock signal on Neighbor 1 and Neighbor 2.

Resistors R1 to R6 represent parasitic resistances along the clock channel. For parallel clock channels, R1 to R6 are poly resistances along the gate transmission line. For the serial lines, metal is used to transmit the serial clock signals instead of poly gate, and R1 to R6 are too small to matter. R7 is the substrate resistance, which is typically 10 ohms.
C2 and C3 are cross-capacitors between the Main Clock signal and the two neighboring signals. Because the substrate is always tied to ground, C1 can be considered as the capacitance between Main Clock and ground. As the cross capacitors between neighbor 1 and 2 are added to their capacitances to ground, we should have:

\[ C_4 = C_5 = C_1 + C_2 \]  \hspace{1cm} (4-2)

Due to the layout of the CCD, we can assume

\[ C_2 = C_3 = \frac{1}{2} C_1 \]  \hspace{1cm} (4-3)

As the model in Figure 4-10 only represents one single pixel, to simulate one the parallel line of the CCD, we need to use the model 4096 times, and connect them one after another. This builds a distributed load, which is difficult to simulate.
However, for the serial clock lines, because R1 to R6 can be ignored, the total load can be considerably simplified.

Figure 4-11 shows the simplified serial clock channel crosstalk model. Figure 4-11 (a) shows the expected load, where CS2 and CS3 represent the total cross-capacitance of the 4096 serial pixels, and CS1, CS4, and CS5 represent the total capacitance from each clock line to ground. Because all of the R7s in Figure 4-10 are in parallel on the serial clock line, the resistance from R7 should be R7/4096, and can be ignored.

The actual capacitance values are derived from the datasheet of the CCD231-84, which is a scientific CCD produced by e2V, and has characteristics comparable with the LSST CCDs. The derived capacitance per line is around
350 pF, so we have CS1 = 175 pF, CS2 = CS3 = 88 pF and CS4 = CS5 = 263 pF.

Due to the space constraints within the temperature chamber, only crosstalk between two serial signals was tested. The third clock signal was assumed to be tied to ground, and the cross capacitor CS3 was added to Clock 1 ground capacitance. Figure 4-11 (b) shows the actual test load setup.

The crosstalk test result is shown in Figure 4-12. Crosstalk between the two clock signals can be clearly observed. To better measure the crosstalk between the two signals, the LVDS input signals are slowed down to 166 kHz with a 120° phase difference. This gives enough time for the overshoot of the signals to settle out and made the measurement more accurate.

Table 4-3 shows the measured crosstalk results of the test, which are higher

![Figure 4-12 CCD Serial Clock Channel Crosstalk Scope Image (I)](image)
than the simulation results. Comparing with the simulation results, the clock signal waveform in the test has overshoot in both the rising and falling edges which is not seen in the simulation. A further simulation shows that the difference is caused by the parasitic inductance from the long wires connecting the power supply to the test boards. As the SCC will be very close to the CCD and power supply in the real application, which would have much less parasitic inductance, we can rightfully expect a final result with less crosstalk.

A further crosstalk test with 1-MHz LVDS inputs is shown in Figure 4-13. The long settling time, coupled with overshoot for both edges, makes it hard for us to analyze the crosstalk results. Both serial clock waveforms in the crosstalk test are not as clean as in the single serial clock test waveform. The reason for
that includes a different load model, as well as more parasitics from the extra boards and wires.

Figure 4-13 CCD Serial Clock Channel Crosstalk Scope Image (II)
LVDS signal at 1MHz, −100°C
CHAPTER 5
CONCLUSIONS

5.1 Conclusions

This thesis presented the design and analysis of a sensor control chip for the Large Synopsis Survey Telescope fabricated in a high-voltage BCD-SOI process. The ASIC has a high-voltage high-current clock channel, a high-voltage bias channel, and programmable voltage adjusting circuits. It is capable of providing a 20-V adjustable clock signal with a maximum output current of 150 mA for the CCDs. Several techniques have been used to enable flexibility in the design and to reduce the power consumption.

Tests have shown that the ASIC performs as expected in both room temperature and low temperature (−100°C) environments. The prototype chip is fully functional and the test results agree well with simulations. With the robust design of the chip, the user can further adjust the output voltage per bit for the bias channel or the maximum output current for the clock channel, to adjust for the performance of the CCD load.

5.2 Future Work

Although the prototype ASIC is verified to be fully functional and capable for the target application, there are some improvements that need to be made for the next version of the SCC. For example, the asymmetrical behavior between the rising edge and falling edge of the clock signal needs to be addressed in the next
version of the SCC. Also, a more symmetrical common-centroid layout should be made for the DAC to improve its performance.

Additionally, there are discrepancies in the crosstalk test between simulation results and test results. Although most of these come from the parasitics of the test setup, it is desirable to further test the crosstalk with a prototype CCD, once it is available, to fully understand and evaluate the SCC performance.

The next version of the SCC will be designed for the LSST system integration, and will integrate more channels into the chip. A new version of the SCC with five clock channels and five bias channels is currently under development, and is designed to drive each CCD with two SCCs.
LIST OF REFERENCES
LIST OF REFERENCES


[12] Dr. O’Connor, Paul (private communication), 2008


APPENDIX
Figure A-1 SCC Remote Test Board

Figure A-2 Spartan 3 Board (Left) and SCC Interface Test Board (Right)
Figure A-3 Computer (top) and NI Chassis (bottom)

Figure A-4 Complete Test System
VITA

Zuoliang Ning was born in Dalian, China on November 29, 1983. He grew up in Dalian, and graduated from Dalian Yu Ming High School in 2001. Then Zuoliang entered Harbin Institute of Technology, and graduated with a Bachelor’s degree in Control Science and Technology in 2005.

After his graduation, Zuoliang worked as an intern in the Microelectronics Laboratory, Dalian University of Technology for one year. In Fall 2006, he entered the University of Tennessee to study for his Master of Science degree in Electrical Engineering. He worked as a Research Assistant in the Integrated Circuits and Systems Laboratory (ICASL) under the direction of Dr. Benjamin Blalock since May 2007. Within the research group, Zuoliang was awarded the opportunity to work with Dr. Charles Britton, Jr. and Dr. Nance Ericson from the Oak Ridge National Laboratory while fulfilling his research requirements for his Master’s degree.